REMARKS

Claims 1-15 remain pending in this application. Of these claims, claims 1-3 and 5 stand rejected under 35 USC §103(a) as being unpatentable over Zubrzycki et al. Claims 4, 6 and 7 stand rejected under 35 USC §103(a) as being unpatentable over Zubrzycki et al. in view of the admitted prior art and Joannopoulos et al. Claims 8-15 stand rejected under 35 USC §103(a) as being unpatentable over Zubrzycki in view of Scherer et al. Claims 1-5 and 7-10 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-11 of U.S. Patent No. 6,649,439. Claims 5, 6 and 11-15 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-11 of U.S. Patent No. 6,649,439 in view of Applicant's admitted prior art, Zubrzycki et al. and Scherer et al.

In view of the following remarks, these rejections are traverse, and reconsideration of this application is respectfully requested.

The parent application Serial No. 10/210,799 is now U.S. Patent No. 6,649,439. The '799 application was the subject of a restriction requirement per the Examiner's Amendment and comment mailed with the Notice of Allowability in paper no. 4. The claims of this application are directed to the non-elected restricted claims 12-21 that were cancelled by the Examiner's Amendment. Applicant respectfully submits that pursuant to MPEP 804.01 and 35 USC §121, the Examiner is prohibited from rejecting the claims in this application under obviousness-type double patenting in view of U.S. Patent No. 6,649,439. Particularly, 35 USC §121 prohibits the use of a patent issuing on an application with respect to which a requirement for restriction has been made as a reference against any divisional application. Therefore, it is respectfully requested that the obviousness-type double patenting rejections be withdrawn.

U.S. Patent No. 6,365,428 issued to Zubrzycki et al. was filed June 15, 2000 and issued April 2, 2002. Applicant reserves the right to file a §1.131 Affidavit swearing behind this reference if a Final Rejection is mailed that rejects Applicant's claims in view of this reference.

Applicant's invention is a method of fabricating an optical diffraction device. Independent claim 1 includes growing a first semiconductor layer on a semiconductor substrate, depositing a dielectric layer on the first semiconductor layer, patterning and etching the dielectric layer to form openings in the dielectric layer to expose selective areas in the first semiconductor layer and to create diffraction regions made out of the dielectric material, and growing a second semiconductor layer by an epitaxial growth process on the first semiconductor layer between the dielectric diffraction regions. Independent method claims 8 and 15 further include etching access vias through the second semiconductor layer to expose the dielectric diffraction regions, and etching away the diffraction region material to define the diffractions regions out of air.

Applicant respectfully submits that the prior art of record does not teach or suggest these claimed methods.

Zubrzycki et al. discloses an embedded distributed grating structure. The grating structure is fabricated by growing a GaAs semiconductor lower index layer 201 on a substrate 200, growing an AlAs semiconductor grating layer 202 on the index layer 201, using an etch mask 203 to pattern and etch the grating layer 202 to define grating elements 204 made of AlAs, and growing a GaAs upper index layer 206 over the grating elements 204 to define the optical structure.

As the Examiner correctly notes, Zubrzycki et al. fails to teach that the grating layer 102, 202 is a dielectric layer. However, it is the Examiner's position that it would have been

obvious to deposit a dielectric layer instead of growing the semiconductor grating layer 102, 202 because Zubrzycki et al. teaches dielectric elements in a grating layer, citing column 2, lines 27-35, recreated below.

> A more recent approach aims to obtain high-contrast unfilled distributed grating structures by using air as the second grating material. These are often called surface gratings, and are formed by growing a suitable dielectric layer, then defining and etching a pattern of deep open trenches in the surface of that layer. The trenches must be quite deep so that the optical mode of interest does not strongly interact with the trench's open ends, the result of which would be large diffraction and scattering losses. (emphasis added)

Applicant respectfully submits that the Examiner has improperly combined the teachings of Zubrzycki et al. to hold that Applicant's claims are *prima facie* obvious. The dielectric grating layer discussed in column 2 above is a surface grating deposited and patterned on a top surface of the optical device. The optical structure claimed by Applicant and described in the Zubrzycki et al. figures 1 and 2 include an embedded diffraction layer. There is no suggestion or teaching in Zubrzycki et al. of depositing a dielectric layer to provide the diffraction grating layer 202 that is then etched to define dielectric grating elements 204. Contrary, Zubrzycki et al. only teaches that the embedded grating is a semiconductor layer that is grown on the index layer 202. The surface grating layer taught by Zubrzycki et al. is a deposited dielectric layer, but there is no teaching or suggestion to also grow a second semiconductor layer over the deposited dielectric layer.

Applicant's claimed invention is a method of fabricating an optical diffraction device that includes specific and sequenced method steps. Applicant submits that the device fabrication processes for growing and etching an embedded semiconductor diffraction grating and the device fabrication processes for depositing and etching a surface dielectric

diffraction grating are different and unobvious than the fabrication processes for depositing and etching an embedded dielectric diffraction grating. Therefore, Applicant respectfully submits that it is improper to hold that the embedded semiconductor grating layer taught by Zubrzycki et al. can be a dielectric layer as claimed by Applicant under *prima facie* obviousness.

Independent method claims 8 and 13 further include providing access vias through the second semiconductor layer to expose the dielectric diffraction regions, and then etching the dielectric diffraction regions through the vias to removed the dielectric material to form the diffraction regions out of air. Applicant's claimed method of fabricating embedded diffraction regions of air includes inherent process steps for an optical grating. For example, it is necessary to provide the access vias away from the active region of the optical device so that device performance is not affected.

It is believed that the Examiner is relying on Scherer et al. to teach this feature of Applicant's invention. Scherer et al. discloses an optical device including a pattern of holes 24 formed through semiconductor layers 18. Conventional wet or dry etching techniques are used to create an undercut air region 28 do make the layer 18 a freestanding membrane for a two-dimensional, photonic crystalline semiconductor cavity.

Applicant respectfully submits that Scherer et al. does not teach or suggest creating embedded diffraction regions of air by etching dielectric diffraction regions through access vias. Applicant submits that Scherer et al. does not teach that the undercut air region 28 is a diffraction region, or that it is a diffraction region from which a dielectric material has been removed. Applicant further submits that there is no suggestion or motivation in either Zubryzcki et al. or Scherer et al. that etching an already embedded dielectric diffraction region can be used in a process for fabricating an optical diffraction device. Therefore,

Applicant submits that Scherer et al. fails to provide the teaching missing from Zubrzycki et al. to make Applicant's independent method claims 8 and 13 obvious.

U.S. Patent No. 5,955,743 issued to Joannopoulos et al. discloses a light emitting device. It is believed the Examiner is relying on Joannopoulos et al. to teach forming two semiconductor layers having different refractive indices for the benefit of forming integrated light emitting devices. However, Applicant submits that Joannopoulous et al. fails to provide the teachings missing from Zubrzycki et al. and Scherer et al. of embedded dielectric diffraction regions and removing embedded dielectric diffraction regions that could be used to make independent claims 1, 8 and 13 obvious as discussed above.

In view of the discussion above, it is respectfully requested that the §103(a) rejections be withdrawn.

It is now believed that this application is in condition for allowance. If the Examiner believes that personal contact with Applicant's representative would expedite prosecution of this application, he is invited to call the undersigned at his convenience.

Respectfully submitted,

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Date: 7/16/04

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